10/625061

TJW

AMENDMENTS TO THE CLAIMS

In the Claims:

Please amend the Claims, as follows:

Claims 1-19. (Cancelled)

20. (New) A method comprising:

consecutively receiving at and writing into a memory a sequence of groupings of bits from a data stream, the groupings of bits having a predetermined size;

reading from the memory a subset of the sequence of the groupings written into the memory, the subset having fewer groupings of bits than the sequence of groupings of bits written into the memory;

applying the subset to a first multiplexer (MUX);

applying another data stream to a second MUX, the another data stream comprising bits representing a virtual local area network (VLAN) tag; and

selectively applying to a third MUX the subset applied to the first MUX and another data stream applied to the second MUX.

21. (New) The method of claim 20, wherein:

the memory comprises a first in, first out (FIFO) memory; and

the reading is based upon a read pointer generated by a state machine.

22. (New) The method of claim 21, wherein:

the state machine also generates a first MUX select signal, a second MUX select signal, and a third MUX select signal applied to the first MUX, the second MUX, and the third MUX, respectively.

23. (New) An apparatus comprising:

a memory capable of consecutively receiving and storing a sequence of groupings of bits

from a data stream, the groupings of bits having a predetermined size, the memory also being capable of retrieving a subset of the sequence of the groupings written into the memory, the subset having fewer groupings of bits than the sequence of groupings of bits written into the memory; and

a first multiplexer (MUX), a second MUX, and a third MUX;

the apparatus being capable of applying the subset to the first MUX, applying another data stream to the second MUX, and selectively applying to a third MUX the subset applied to the first MUX and another data stream applied to the second MUX, the another data stream comprising bits representing a virtual local area network (VLAN) tag.

24. (New) The apparatus of claim 23, wherein:

the memory comprises a first in, first out (FIFO) memory; and

the apparatus also comprises a state machine to generate a read pointer, the memory being capable of retrieving the subset based upon the read pointer.

25. (New) The apparatus of claim 24, wherein:

the state machine is also capable of generating a first MUX select signal, a second MUX select signal, and a third MUX select signal to be applied to the first MUX, the second MUX, and the third MUX, respectively.

26. (New) A system comprising:

an integrated circuit comprising:

a memory capable of consecutively receiving and storing a sequence of groupings of bits from a data stream, the groupings of bits having a predetermined size, the memory also being capable of retrieving a subset of the sequence of the groupings written into the memory, the subset having fewer groupings of bits than the sequence of groupings of bits written into the memory; and

a first multiplexer (MUX), a second MUX, and a third MUX;

the integrated circuit being capable of applying the subset to the first MUX, applying another data stream to the second MUX, and selectively applying to a third MUX the subset applied to the first MUX and another data stream applied to the second MUX, the another data stream comprising bits representing a virtual local area network (VLAN) tag.

27. (New) The system of claim 26, further comprising:

an input data bus coupled to the memory.